

**Amendment to the Specification:**

Please replace the paragraph on page 3, line 32, with the following new paragraph:

The signal to the valve 8 is produced using control and converter circuitry ~~as shown in FIGS. 4-60~~ that operates as follows. An incoming pulse train arrives at the input to a bidirectional optical isolator (IN1). The coupled signal becomes OUT1. The output of the buffer, a 5V logic level version of the input signal, is fed into a processor. The processor calculates an input duty cycle by measuring the pulse width and frequency of the incoming signal. From this, the constant on-time frequency is calculated, and the information is transferred to a set of valve drivers. The processor then calculates a duty cycle according to the formula  $[DC = \text{Pulse Width} \times \text{Frequency}]$ . The processor uses this same formula to create an output with equal or scaled duty cycle utilizing a pre-defined pulse width and a calculated frequency.